REMARKS

This Amendment responds to the final Office Action mailed October 28, 2008, in the above-identified Application. The foregoing amendments do not raise new issues or require extensive consideration. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1–3, 6–15 and 18–24 are currently pending in the application. By this Amendment, claims 1, 3, 6, 7, 10, 12, 13, 15, 18, 19, 22 and 24 have been amended. The amendments find clear support in the original application at least in Fig. 4 and the corresponding description at page 10, line 18 to page 11, line 16. No new matter has been added.

The Examiner has rejected claims 1–3, 6, 7, 9–15, 18, 19 and 21–24 under 35 U.S.C. §103(a) as unpatentable over Levin (U. S. 6,639,906) in view of Sato (U.S. 5,982,763) and Bultan et al. (U.S. 7,206,335). Claims 8 and 20 are rejected under 35 U.S.C. §103(a) as unpatentable over Levin in view of Sato and Bultan et al. as applied to claims 1 and 13, further in view of Komatsu (U.S. 6,816,542). The rejections are respectfully traversed for the following reasons.

Levin describes a system for performing digital receive processing for multiple signals received over the same RF band (col. 3, lines 27-29). A demodulator shown in Fig. 5 includes XOR banks 204-210 which generate offset despread data (col. 8, lines 29-39). An early interpolation circuit 212, an on-time interpolation circuit 214 and a late interpolation circuit 216 interpolate the outputs of XOR banks 204-210 (col. 8, line 66 to col. 9, line 30). The Examiner concedes that Levin fails to disclose, after completion of the despreading, interpolating the two or more despread results including selecting interpolation coefficients based on the previously estimated finger location.

Bultan describes a digital timing synchronizer of a receiver for timing synchronization to a transmitter in a wireless communication system, wherein the received signal has a timing error with respect to a reference code. A channel estimator estimates an initial code phase of the

received signal. A code generator generates a timing reference code that is adjustable by integer increments. An interpolation feedback circuit is configured for interpolation and correction of the timing error, whereby the interpolation is achieved through an integer code shift, plus a quantized fractional delay estimate selected from a look-up table of quantized values of fractional delay estimates associated with predetermined interpolator coefficients, from which a time corrected version of the signal is produced (col. 2, lines 14-27). Bultan describes chip rate interpolation rather than interpolation after completion of despreading, as is apparent from the fact that received signal 21 is provided directly to interpolator 14 in Fig. 1. Furthermore, Bultan indicates that the timing error estimate is in a range of $-T_c$ to T_c, where T_c is the duration of one chip period (col. 3, lines 18-35).

The Examiner contends that it is implicit that the coefficients of Bultan correspond to a "previously estimated finger location", since the delayed output by interpolator 14 is fed back to the timing error estimator and the process is repeated. Applicant must respectfully disagree. The cited portion of Bultan at col. 8, lines 26-29 states that the delay estimation and interpolation operation is continuously repeated to track changes in the timing error. However, tracking changes in a timing error is very different from performing interpolation using selected despread results and selected interpolation coefficients to provide an estimated symbol value at the previously estimated finger location, as required by amended claim 1. Nowhere does Bultan disclose or even remotely suggest performing interpolation to provide an estimated symbol value at a previously estimated finger location.

Sato discloses a reception timing detection circuit of a CDMA receiver including an A/D converter for obtaining a digital reception signal, a correlator for obtaining a cross-correlation between the digital reception signal and a known signal series periodically within a predetermined lag and an interpolation filter for resampling the signal output from the correlator at a frequency higher than a sampling frequency for the A/D converter (Abstract and Fig. 1). The interpolation filter interpolates a correlation value between two samples per chip from the correlator so as to calculate the correlation value with higher delay accuracy. An example for

obtaining a cross-correlation value with an accuracy of 1/8 chip is shown in Figs. 3A to 3C of Sato (col. 5, line 56 to col. 6, line 5). Thus, Sato discloses chip rate interpolation and does not disclose performing interpolation to provide an estimated symbol value at a previously estimated finger location.

It is submitted that Levin, Bultan and Sato, taken individually or in combination, do not disclose or suggest *selecting, from the two or more despread results, despread results near a previously estimated finger location, selecting interpolation coefficients based on the previously estimated finger location, and performing interpolation using the selected despread results and the selected interpolation coefficients to provide an estimated symbol value at the previously estimated finger location*, as required by amended claim 1. While the cited references describe despreading and interpolation in connection with processing a spread spectrum signal, none of the cited references even remotely describes performing interpolation as defined by amended claim 1. Accordingly, the skilled person would not be led by the combined teachings of the cited references to provide the claimed method for processing a spread spectrum baseband signal. For at least these reasons, amended claim 1 is clearly and patentably distinguished over Levin in view of Sato and Bultan, and withdrawal of the rejection is respectfully requested.

Claims 2, 3 and 6-12 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Amended claim 13 is directed to apparatus for processing a spread spectrum baseband signal and contains apparatus limitations that parallel the method limitations of claim 1. As should be apparent from the discussion above, amended claim 13 is clearly and patentably distinguished over Levin in view of Sato and Bultan, and withdrawal of the rejection is respectfully requested.

Claims 14, 15 and 18-23 depend from claim 13 and are patentable over the cited references for at least the same reasons as claim 13.

Amended claim 24 is directed to apparatus for processing a spread spectrum baseband signal comprising a digital signal processor including a memory, a program sequencer and at least one computation block for executing an instruction sequence. The computation block includes circuitry for executing a process as defined by claim 1. As should be apparent from the discussion above, amended claim 24 is clearly and patentably distinguished over Levin in view of Sato and Bultan, and withdrawal of the rejection is respectfully requested.

Based upon the above discussion, entry of the Amendment and allowance of the application are respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary one month extension of time. The fee is occasioned by this response, including the one month extension fee, if not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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